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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 10

| *Complete if Known* | |
|---|---|
| Application Number | 10/757,939 |
| Filing Date | January 16, 2004 |
| First Named Inventor | Craig C. HANSEN, et al. |
| Group Art Unit | 2183 |
| Examiner Name | CHAN, EDDIE P |
| Attorney Docket Number | 43876-153 |

**U.S. PATENT DOCUMENTS**

| Examiner Initials* | Cite No.[1] | Document Number Number-Kind Code[2] (*if known*) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|
| | AA | US-4,852,098 | 07/25/1989 | Brechard, et al. | |
| | AB | US-4,875,161 | 10/17/1989 | Lahti, et al. | |
| | AC | US-4,949,294 | 08/14/1990 | Wambergue, et al. | |
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|---|---|---|---|---|---|---|
| | AT | WO 93/11500 | | | | |

| Examiner Signature | | Date Considered | 4/10/06 |
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| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 2 | of | 10 | Attorney Docket Number | 43876-153 |

| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | |
|---|---|---|---|
| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T[2] |
| HC | AU | IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563) | |
| | AV | IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529) | |
| | AW | Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 –848) | |
| | AX | IBM, "The PowerPC Architecture: A Specification For A New Family of RISC Processors," 2nd Ed., Morgan Kaufmann Publishers, Inc., (1994) (50006DOC019229 – 767) | |
| | AY | Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228) | |
| | AZ | MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621) | |
| | BA | i860™ Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn | |
| | BB | Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900) | |
| | BC | Gove, "The Multimedia Video Processor (MVP): A Chip Architecture for Advanced DSP Applications," IEEE DSP Workshop, pp. 27-30 (October 2-5, 1994) (51056DOC015452 – 455) | |
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| | BI | Bowers et al., "Development of a Low-Cost, High Performance, Multiuser Business Server System," Hewlett-Packard Journal, Vol. 46, No. 2, p. 79 (April 1995) (51056DOC059277 – 282) | |
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| | BL | Kurpanek et al., "PA7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156) | |
| | BM | Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167) | |
| HC | BN | Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557) | |

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|---|---|---|---|---|---|
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| | BQ | US-5,734,874 | 03/31/1998 | Van Hook, et al. | |
| | BR | US-5,758,176 | 05/26/1998 | Agarwal, et al. | |
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| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | |
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| | BY | Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090) | |
| | BZ | Undy et al., "A Low-Cost Graphics and Multimedia Workstation Chip Set," IEEE Micro, pp. 10-22 (April 1994) (51056DOC002578 – 590) | |
| | CA | HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141) | |
| | CB | PA-RISC 1.1 Architecture and Instruction Set Reference Manual, Third Edition, Hewlett-Packard (February 1994) (51056DOC002157 – 176) | |
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| | CD | Beckerle, "Overview of the StarT (*T) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519) | |
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| | CL | R. Mueller, "The MC88110 Instruction Sequencer," Northcon, 1992 (51056DOC009735 – 738) | |
| | CM | J. Arends, "88110: Memory System and Bus Interface," Northcon, 1992 (51056DOC009739 – 742) | |
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| | CO | J. Maguire, "MC88110: Datpath," Northcon, 1992 (51056DOC010059 – 063) | |
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| | CQ | Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661) | |
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## OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

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|---|---|---|---|
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| | CV | Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 – 607) | |
| | CW | Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291) | |
| | CX | Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 -034) | |
| | CY | Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 – 279) | |
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| | DE | Wadleigh et al., "High Performance FFT Algorithms for the Convex C4/XA Supercomputer," Poster, Conference on Supercomputing, Washington, D.C. (November 1994) (51056DOC068618) | |
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| | DI | "Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390) | |
| | DJ | Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993) | |
| | DK | Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598) | |
| | DL | Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236) | |
| | DM | Saturn Overview (November 12, 1993) (51056DOC017111 - 157) | |
| | DN | Convex Notebook containing various "Machine Descriptions" (51056DOC016994 – 7510) | |
| | DO | "Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383) | |
| | DP | Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 – 443) | |
| | DQ | Excerpt from "Advanced Computer Architectures - A Design Space Approach," Chapter 14.8, "The Convex C4/XA System" (51056DOC061453 – 459) | |
| | DR | Convex C4600 Assembly Language Manual, First Edition, May 1995 (51056DOC064728 – 5299) | |
| | DS | Alvarez et al., "A 450MHz PowerPC Microprocessor with Enhanced Instruction Set and Copper Interconnect," ISSCC (February 1999) (51056DOC071393 - 394) | |

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|---|---|---|---|
| | DT | Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042) | |
| | DU | AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392) | |
| | DV | Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 – 666) | |
| | DW | Grimes et al., "A New Processor with 3-D Graphics Capabilities," NCGA '89 Conference Proceedings Vol. I, pp. 275-84 (April 17-20, 1989) (5156DOC070711 – 717) | |
| | DX | Grimes et al., "The Intel i860 64-Bit Processor: A General-Purpose CPU with 3D Graphics Capabilities," IEEE Computer Graphics & Applications, pp. 85-94 (July 1989) (5156DOC070701 – 710) | |
| | DY | Kohn et al., "A 1,000,000 Transistor Microprocessor," 1989 IEEE International Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, 290 (February 15, 1989) (51056DOC072091 – 094) | |
| | DZ | Kohn et al., "A New Microprocessor with Vector Processing Capabilities," Electro/89 Conference Record, pp. 1-6 (April 11-13, 1989) (5156DOC070672 – 678) | |
| | EA | Kohn et al., "Introducing the Intel i860 64-Bit Microprocessor," IEEE Micro, pp. 15-30 (August 1989) (5156DOC070627 – 642) | |
| | EB | Kohn et al., "The i860 64-Bit Supercomputing Microprocessor," AMC, pp. 450-56 (1989) (51056DOC000330 – 336) | |
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| | ED | Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 – 700) | |
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| | EF | Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 – 647) | |
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| | EH | Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 – 101) | |
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| | EK | N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982) | |
| | EL | N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551) | |
| | EM | N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509) | |
| | EN | N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441) | |
| | EO | N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851) | |
| | EP | N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 – 73027) | |
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| | ER | Moussouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 – 630) | |

| Examiner Signature | | Dated Considered | 4/10/06 |
|---|---|---|---|

*EXAMINER: Initial reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached. This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P. O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORM TO THIS ADDRESS. **Send To Commissioner For Patents, P. O. Box 1450, Alexandria, VA 22313-1450.** If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2

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| Substitute for form 1449B/PTO | | | | Complete if Known | |
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| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** | | | | Application Number | 10/757,939 |
| | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| *(use as many sheets as necessary)* | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 7 | of | 10 | Attorney Docket Number | 43876-153 |

| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | |
|---|---|---|---|
| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T[2] |
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| | EU | Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 – 040) | |
| | EV | Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 – 300) | |
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| | FA | Giloi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801) | |
| | FB | Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 – 673) | |
| | FC | Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662) | |
| | FD | Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028) | |
| | FE | Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694) | |
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| Examiner Signature | | Dated Considered | 4/10/06 |
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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 8 of 10

| Complete if Known | |
|---|---|
| Application Number | 10/757,939 |
| Filing Date | January 16, 2004 |
| First Named Inventor | Craig C. HANSEN, et al. |
| Group Art Unit | 2183 |
| Examiner Name | CHAN, EDDIE P |
| Attorney Docket Number | 43876-153 |

## OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T[2] |
|---|---|---|---|
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| | FO | Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 – 887) | |
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| | FT | Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 – 609) | |
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| | FW | Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 – 443) | |
| | FX | Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 – 256) | |
| | FY | Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 – 936) | |
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| | GB | "Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206) | |
| | GC | Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209) | |
| | GD | Data General AViiON AV500, 550, 4500 and 5500 Servers | |
| | GE | Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779) | |
| | GF | High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801) | |
| | GG | National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 – 243) | |
| | GH | Wilson, "The History of the Development of Parallel Computing," http://ei.cs.vt.edu/~history/Parallel.html (51056DOC068720 - 757) | |

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| **INFORMATION DISCLOSURE STATEMENT BY APPLICANT** | | | | Application Number | 10/757,939 |
| | | | | Filing Date | January 16, 2004 |
| | | | | First Named Inventor | Craig C. HANSEN, et al. |
| *(use as many sheets as necessary)* | | | | Group Art Unit | 2183 |
| | | | | Examiner Name | CHAN, EDDIE P |
| Sheet | 9 | of | 10 | Attorney Docket Number | 43876-153 |

| OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS | | | |
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| Examiner Initials* | Cite No.[1] | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published. | T[2] |
| | GI | IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323) | |
| | | Original Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004 | |
| | GJ | Amended Complaint for Patent Infringement, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004 | |
| | GK | Expert Witness Report of Richard A. Killworth, Esq., *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | |
| | GL | Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005 | |
| | GM | Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005 | |
| | GN | Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005 | |
| | GO | Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005 | |
| | GP | Request for *Inter Partes* Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005 | |
| | GQ | Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | |
| | GR | Deposition of Leslie Kohn on September 22, 2005; *MicroUnity Systems Engineering, Inc. v. Dell, Inc. f/k/a/ Dell Computer and Intel Corporation*; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division | |
| | GS | Intel Article, *"Intel Announces Record Revenue of 9.96 Billion"*, October 18, 2005 | |
| | GT | The New York Times Article, *"Intel Posts 5% Profit Increase on Demand for Notebook Chips"*, October 19, 2005 | |
| | GU | USA Today Article, *"Intel's Revenue Grew 18% In Robust Quarter for Tech"*, October 19, 2005 | |
| | GV | The Wall Street Journal Article, *"Intel Says Chip Demand May Slow"*, October 19, 2005 | |
| | GW | The New York Times Article, *"Intel Settlement Revives A Fading Chip Designer"*, October 20, 2005 | |

| Examiner Signature | | Dated Considered | 4/10/06 |
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# INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

| ATTY. DOCKET NO. | SERIAL NO. |
|---|---|
| **043876-0153** | **10/757,939** |

APPLICANT: **Craig HANSEN, et al.**

| FILING DATE | GROUP |
|---|---|
| **January 16, 2004** | **2183** |

## U.S. PATENT DOCUMENTS

| EXAMINER'S INITIALS | CITE NO. | Document Number Number-Kind Code2 (if known) | | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear |
|---|---|---|---|---|---|---|
| | A | US | 6,643,765 | 11-04-2003 | Hansen et al. | |
| | B | US | 6,725,356 | 04-20-2004 | Hansen et al. | |
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## FOREIGN PATENT DOCUMENTS

| EXAMINER'S INITIALS | CITE NO. | Foreign Patent Document Country Code3-Number 4-Kind Codes (if known) | Publication Date MM-DD-YYYY | Name of Patentee or Applicant of Cited Document | Pages, Columns, Lines Where Relevant Figures Appear | Translation Yes | Translation No |
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## OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

| EXAMINER'S INITIALS | CITE NO. | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | |
|---|---|---|---|
| | C | MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005) | |
| | D | Intel Press Release, "Intel Announces Record Revenue of $9.96 Billion," Santa Clara, CA, 10-18-2005 | |
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| EXAMINER | DATE CONSIDERED |
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| APPLICANT: **HANSEN, C., et al.** | |
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| | APPLICANT HANSEN, C., et al. | |
| | FILING DATE January 16, 2004 | GROUP 2183 |

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| | APPLICANT HANSEN, et al. | |
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(PTO-1449)

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